REMARKS

Claims 1, 3-8, 12-16, and 20-24 remain rejected as being anticipated by Douglas (U.S. Patent No. 6,609,193), claim 2, along with new claims 28-32, remain rejected as being obvious over Douglas, and claims 9-11, 17-19, and 25-27 remain rejected as being obvious over Douglas in view of Joy (U.S. Patent No. 6,507,862).

Independent claim 1 has been amended to include the features of dependent claims 4-8. Claim 9 has been amended to be in independent form and to include the features of dependent claims 10 and 11. Independent claim 12 has been amended to include the features of dependent claims 14-16. Claim 17 has been amended to be in independent form and to include the features of dependent claims 18 and 19. Independent claim 20 has been amended to include the features of dependent claims 22-24. Claim 25 has been amended to be in independent form and to include the features of dependent claims 26 and 27.

Amended independent claim 1 recites "a data forwarding unit comprising a thread ID comparator, wherein the data forwarding unit is configured to forward data from a first pipeline stage having a first thread ID to a second pipeline stage having a second thread ID when the first thread ID is equal to the second thread ID, and to prevent data forwarding when the first thread ID is not equal to the second thread ID."

With "data forwarding," operands which are to be stored by a later pipeline stage in a memory, can additionally be forwarded directly to an earlier pipeline stage, resulting in that the earlier pipeline stage does not have to wait until the operand is written into the memory and to fetch the operand from the memory thereafter. (See paragraphs 6 and 25 of the specification.) The applied prior art documents do not disclose such data forwarding.

Thus claim 1, along with its dependent claims, is patentable over the applied prior art for at least this reason.

Amended independent claim 12, similar to independent claim 1, recites "storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction

from the first set of instructions; forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage; and preventing data forwarding from the first pipeline stage to the second pipeline stage when the first thread ID in the first pipeline stage is not equal to the second thread ID in the second pipeline stage." Thus independent claim 12, along with its dependent claims, is patentable over the applied prior art for at least the same reason as explained above with respect to independent claim 1.

Independent claim 20, similar to independent claims 1 and 12, recites "means for storing the associated thread ID in a thread ID memory in each stage of the pipeline operating on an instruction from the first set of instructions; means for forwarding data from a first pipeline stage to a second pipeline stage when a first thread ID in the first pipeline stage is equal to a second thread ID in the second pipeline stage; and means for preventing data forwarding from the first pipeline stage to the second pipeline stage when the first thread ID in the first pipeline stage is not equal to the second thread ID in the second pipeline stage." Thus independent claim 20, along with its dependent claims, is also patentable over the applied prior art for at least the same reason as explained above with respect to independent claim 1.

Amended independent claim 9 recites "a trap handler configured to resolve a first trap having a first thread ID when the active thread corresponds to the first thread ID, and to suspend the first trap having the first thread ID when the active thread does not correspond to the first thread ID."

Joy does not disclose these features. In view of the fact that the thread switch logic 610 is provided to attain a very fast exception handling functionality while executing non-threaded programs (see Joy, col. 15, lines 8-10), it would not make sense for the processor to be dependent on the thread ID of the active thread, whether or not a trap is executed.

Thus independent claim 9 is patentable over the applied prior art for at least this reason.

Amended independent claim 17, similar to independent claim 9, recites "resolving the trap when the trap thread ID equals the active thread ID; and preventing trap resolution when the trap thread ID does not equal the active thread ID." Thus, independent claim 17 is also patentable over the applied prior art for at least the same reason as explained above with respect to independent claim 9.

Amended independent claim 25, similar to independent claim 9, recites "means for resolving the trap when the trap thread ID equals the active thread ID; and means for preventing trap resolution when the trap thread ID does not equal the active thread ID." Thus, independent claim 25 is also patentable over the applied prior art for at least the same reason as discussed above with respect to independent claim 9.

In view of the above, Applicant believes the pending application is in condition for allowance.

Dated: April 12, 2007

Respectfully submitted,

By Laura C. Brutman

Laura C. Brutman
Registration No.: 38,395
DICKSTEIN SHAPIRO LLP
1177 Avenue of the Americas
41st Floor
New York, New York 10036-2714
(212) 277-6500
Attorney for Applicant